WS No. 19 Mark III

This file has been down loaded from The Wireless-Set-No19 WEB site.

All files from this WEB site are free of charge. If you have been charged for this file then please contact the person you obtained it from as he/she has illegally obtained both the file and money they have charged you.....

ELECTRICAL AND MECHANICAL ENGINEERING REGULATIONS
(By Command of the Army Council)

TELECOMMUNICATIONS
A 339

SEMI-CONDUCTOR CIRCUITS

Errata

Note: This Page 0, Issue 1, will be filed in front of Page 1, Issue 1, dated 5 Oct 62.

1. The following amendments will be made to the regulation.

2. Page 9, para 27, line 3

Delete: 1, 2 and 3
Insert: 1, 2 or 3

Delete: one of the diodes
Insert: the appropriate diode

Distribution - Class 330. Code No 2

3. Page 10, para 29, line 3

Delete: 1, 2 and 3
Insert: 1, 2 or 3

Delete: one of the diodes
Insert: the appropriate diode

4. Page 13, para 37, line 4

Delete: positive
Insert: negative

EME/8e/2146

CONDITIONS OF RELEASE

(Applicable to copies supplied with War Office approval to Commonwealth and Foreign Governments)

1. This document contains classified UK information.

2. This information is disclosed only for official use by the recipient Government and (if so agreed by HM Government) such of its contractors, under seal of secrecy, as may be engaged on a defence project. Disclosure or release to any other Government, national of another country, any unauthorized person, the Press, or in any other way would be a breach of the conditions under which the document is issued.

3. This information will be safeguarded under rules designed to give the same standard of security as those maintained by HM Government in the UK.

SEMI-CONDUCTOR CIRCUITS

SUBJECT INDEX

SUBJECT INDEX - (cont)

GATING CIRCUITS

SIGNAL PROCESSING CIRCUITS

DC/DC CONVERTER CIRCUITS

INDEX TO FIGURES

INDEX TO FIGURES - (cont)

INTRODUCTION

1. This is the second of a series of three EMERs dealing with semi-conductor devices, division of the series is as follows:-

(a) Tels A 018 A series of brief descriptions, each one dealing with a distinct kind of semi-conductor device. No reference will be made to any individual type. This section will be kept up to date by the issue of additional sheets, as new kinds become available.

(b) Tels A 339 Description and examples of basic circuits involving the use of semi-conductor devices.

(c) Tels A 412 The elements of servicing, and techniques peculiar to circuits using semi-conductor devices.

MULTIVIBRATOR TYPE CIRCUITS

BASIC ASTABLE CIRCUIT

General

2. Fig 1 shows a basic astable circuit. This circuit is a self starting, free running pulse generator which switches between two unstable states at a frequency determined mainly by the coupling components. The multivibrator may be triggered by an external source provided that the trigger frequency is the same as, or only slightly higher than, the 'natural' frequency of the multivibrator. The multivibrator may also be used for frequency division by using a circuit with a 'natural' frequency which is an even sub-multiple of the trigger frequency.

Operation

3. When the circuit is switched on, slight component unbalance causes it to go into one or other of the unstable states. It is assumed that a cycle starts with VT1 conducting and VT2 biased off.

VT1 conducts,
Causing voltage drop across R1
C1 charges via VT1 and R2
Voltage drop across R2
VT2 base kept positive
C1 fully charged
VT2 base driven negative
VT2 biased on, conducts
VT2 collector and VT1 base go positive
VT1 biased off
C1 discharges through R1 and VT2
Voltage drop across R4
C2 charges via VT2 and R3
Voltage drop across R3
VT1 base kept positive
C2 fully charged
VT1 base driven negative
VT1 biased on, conducts
VT1 collector and VT2 base go positive
VT2 biased off
C2 discharges through R4 and VT1

4. This cycle of events is repeated continuously, and if time constants, C1R2 and C2R3 are equal, the output waveform is symmetrical.

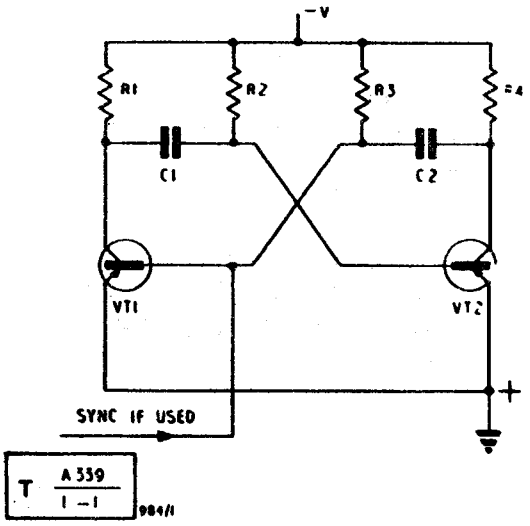


Fig 1 - Basic astable circuit

Practical circuit

A practical astable circuit with component values, is shown in Fig 2. This circuit would function with a pulse repetition frequency (p.r.f.) of about 5kc/s, the output being taken from the collector of either VT1 or VT2. The output waveform would be nearly rectangular with equal mark space ratio.

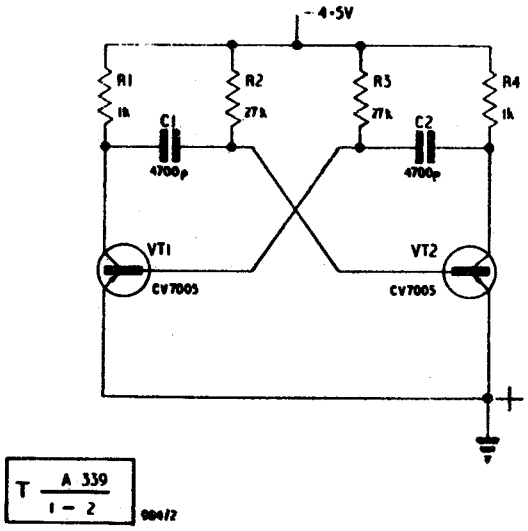


Fig 2 - Practical astable circuit

BASIC MONOSTABLE CIRCUIT (FLIP FLOP)

General

6. Fig 3 shows a basic monostable circuit. This circuit delivers one output pulse for each input pulse. It is switched from the normal stable state into an unstable condition by a trigger pulse, the recovery period being determined mainly by the time constant C2R3. The monostable circuit may be used for pulse amplification, pulse shaping, or as a delay circuit.

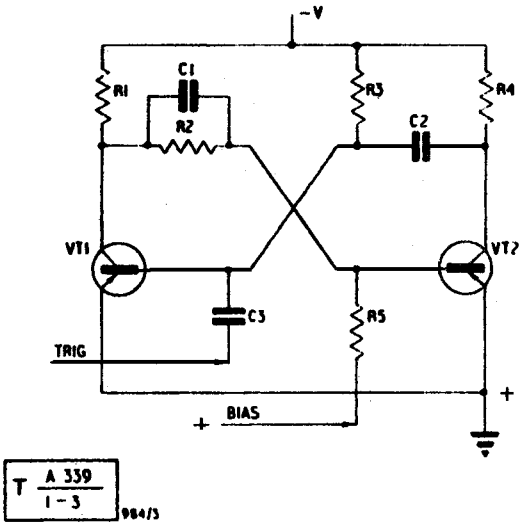


Fig 3 - Basic monostable circuit

Operation

7. The circuit is switched on and assumes a stable state with VT1 conducting and VT2 biased off.

Positive trigger pulse applied to C3
Making VT1 base positive
Biasing VT1 off
Making VT1 collector negative
Making VT2 base negative
VT2 conducts
C2 discharges through R3, VT2
VT1 base becomes negative
VT1 conducts
Making VT1 collector positive
Making VT2 base positive
Biasing VT2 off

8. The circuit remains in this state until triggered again. The capacitor C1 shunting R2, compensates for the attenuation caused by the input capacitance of VT2; thus speeding up switching at high p.r.f.

Practical circuit

9. A practical monostable circuit with component values, is shown in Fig 4. The trigger pulse width has to be greater than the switching time, which in the case of the example shown is about 5μsec. The output may be taken from the collector of either VT1 or VT2.

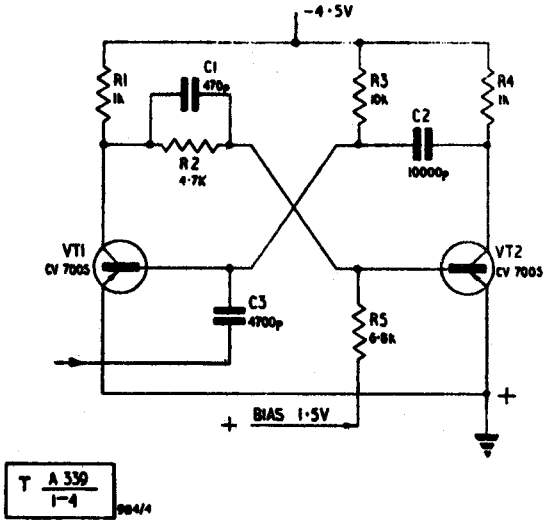


Fig 4 - Practical monostable circuit

BASIC BISTABLE CIRCUIT (ECCLES-JORDAN)

General

10. Fig 5 shows a basic bistable circuit. This circuit has two stable states:- VT1 conducting and VT2 out off; or, VT2 conducting and VT1 cut off.

11. The application of a trigger pulse will switch the circuit from one stable condition to the other. If a series of trigger pulses is applied to alternate transistor bases, the output from either collector, will have a p.r.f. equal to half that of the trigger frequency.

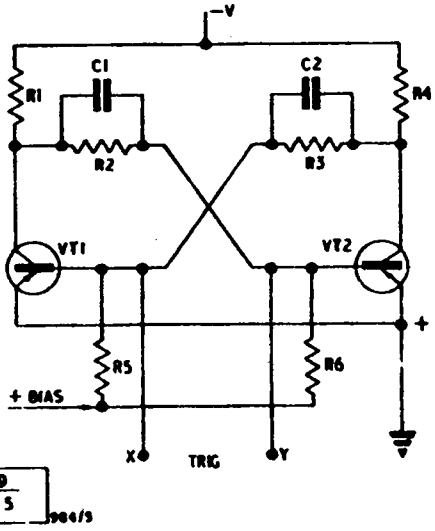


Fig 5 - Basic bistable circuit

Operation

12. The circuit is assumed to be operating with VT1 conducting and VT2 cut off.

Positive trigger pulse applied to X
Making VT1 base positive
Biasing VT1 off
Making VT1 collector negative
Making VT2 base negative
Biasing VT2 on
Making VT2 collector positive
Making VT1 base positive
Maintaining VT1 biased off

13. This state is maintained until a positive trigger pulse is applied to Y, in which case VT1 is switched on and VT2 is switched off, by a similar sequence of events.

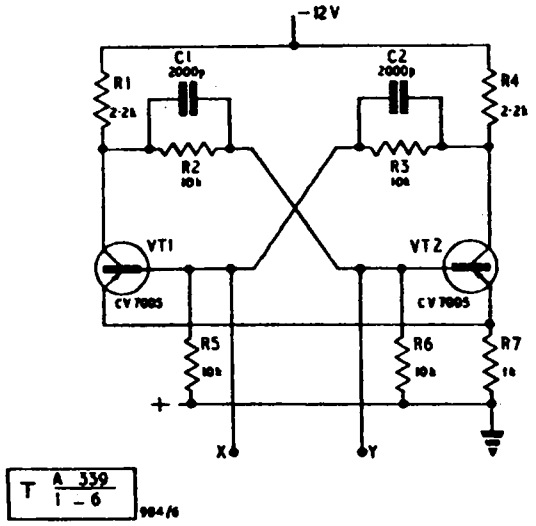


Fig 6 - Practical bistable circuit

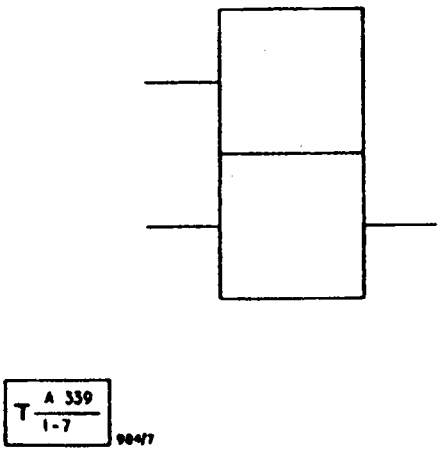


Fig 7 - Bistable element symbol

Practical circuit

14. A practical bistable circuit with component values is shown in Fig 6. Fig 7 shows the symbol used to represent a bistable element in block schematic diagrams.

SCHMITT TRIGGER CIRCUIT

General

15. The Schmitt trigger circuit produces two output pulses, in opposite phase, from a single input pulse. In the circuit shown in Fig 8, output 1 would be in phase with the input, whilst output 2 would be in opposite phase.

Operation

16. VT1 base made negative
VT1 conducts
Making VT2 base negative
VT2 conducts
Making VT3 base positive
VT3 biased off
VT1 base made positive
End of input pulse
VT1 biased off
VT2 biased off
VT2 collector negative
VT3 biased on, conducts
VT1 base returns to negative state
VT1 conducts
VT2 biased on, conducts
VT3 biased off

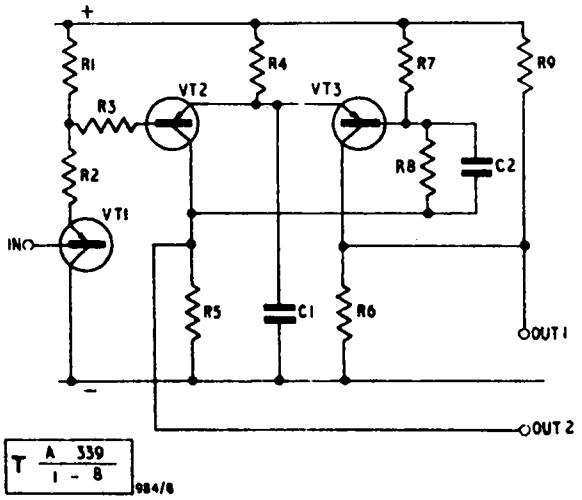


Fig 8 - Basic Schmitt trigger circuit

17. In practice, VT2 and VT3 collector currents cannot be zero, since there is some leakage current, but this is of a very small order.

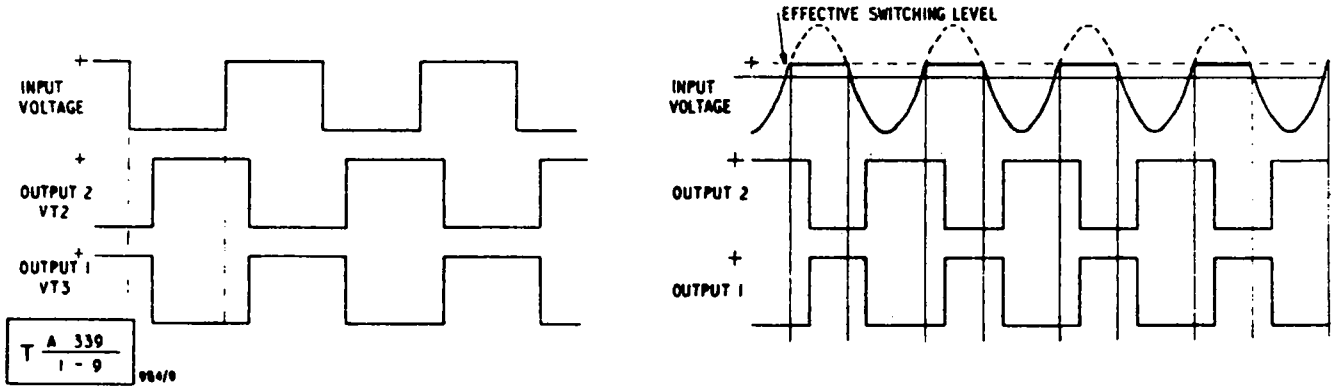


Fig 9 - Schmitt trigger circuit - input and output waveforms

18. There will be a slight time lag between input and outputs, since the transistors have a finite rise time; capacitor C2 is included to keep this rise time as small as possible by ensuring that switching transients are quickly passed to the base of VT3.

19. The output waveform is almost rectangular, but may have any mark space ratio, depending on the nature of the input waveform. Typical examples are shown in Fig 9. If it is essential that the outputs be accurately equal and opposite, then transistor impedances are as important as component values, in design considerations.

Practical circuit

20. Fig 10 shows a practical Schmitt trigger circuit with component values. It will be noted that C1 has a large value (1μF) in order to provide effective decoupling of the common load resistor R4.

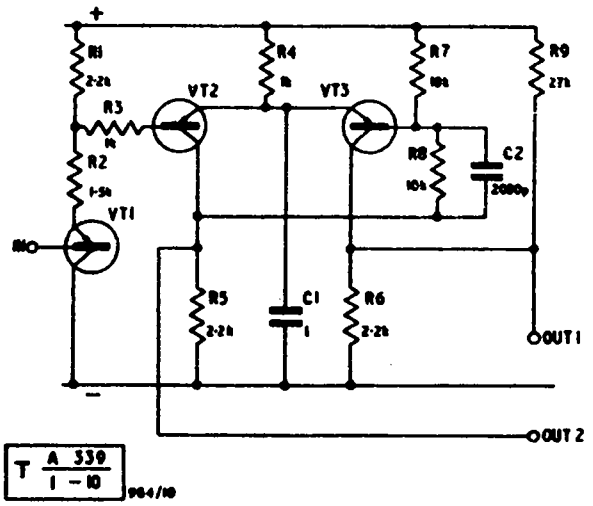


Fig 10 - Practical Schmitt trigger circuit

GATING CIRCUITS

General

21. A gate or gating circuit provides an output when a particular input condition is present. This input condition usually involves the inter-relationship of several input signals.

22. The following examples show the type of circuits employed, and the corresponding logic symbols. In some cases two logic symbols are shown to represent one logic function; such symbols are alternatives and either may be used. The first four examples (para 24-31) each use one transistor, two resistors and three diodes. These components are arranged in different configurations to perform different positive logic functions. That is, input signals and output conditions are positive with respect to negative earth. The same circuits could be rearranged to perform similar functions in negative logic, with positive earth.

23. A logic function may be performed by many different circuit arrangements. The second group of examples (para 32-38) shows some of the more complex, special purpose gating circuits.

AND-gate

(Fig 11)

24. An AND-gate will only produce an output when all inputs are present.

25. In the no signal state, the inputs are negative so that the diodes are conducting and the transistor is biased on. A positive signal applied to point 1, 2 or 3 will bias the appropriate diode into non-conduction but will make no significant difference to the current flowing through the transistor. If positive signals are applied to points 1, 2 and 3 simultaneously, all the diodes will be reverse biased, and the transistor will cease to conduct for the duration of the signals. The positive output condition can therefore only exist if all inputs are energised.

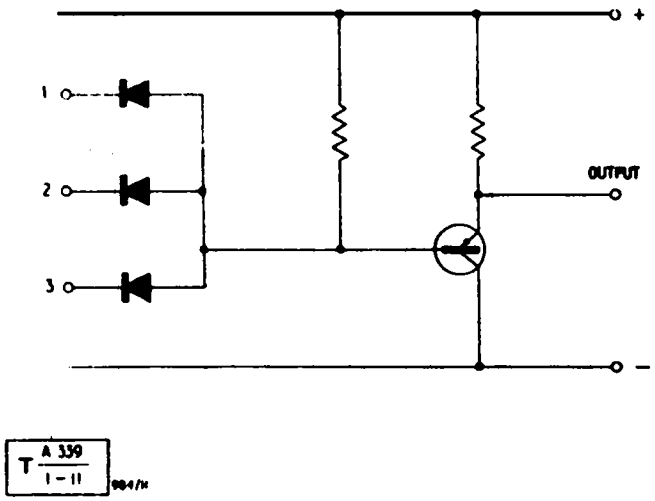


Fig 11A - AND-gate circuit

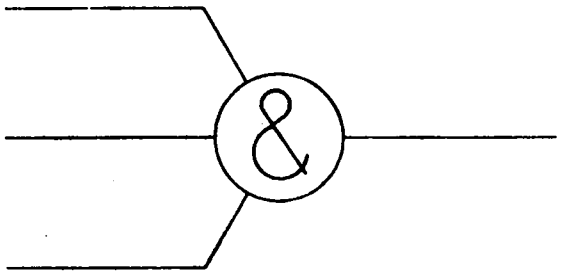


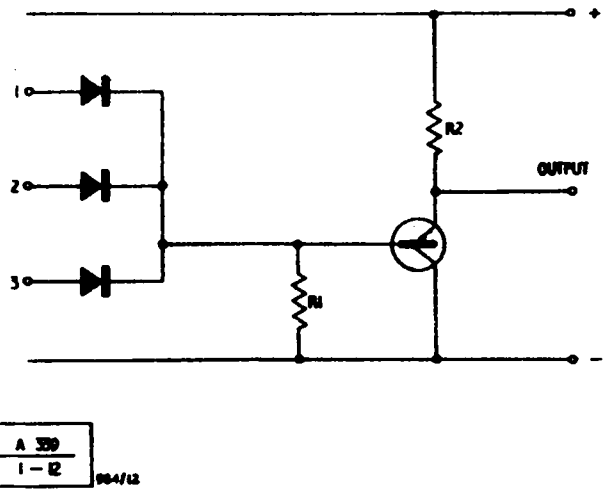
Fig 11B - AND-gate logic symbol

INCLUSIVE OR-gate

(Fig 12)

26. An INCLUSIVE OR-gate will produce an output when at least one input is present.

27. In the no signal state, the inputs are negative so that the diodes are not conducting. The transistor is biased on by base current flowing through R1. A positive signal applied to point 1, 2 and 3 will be conducted through one of the diodes, making the transistor base positive. This will reduce the current flowing through the transistor and hence through R2. Whether one or more inputs are energised at the same time, the result will be the same, and may be detected as a positive output condition.



T A 339 / 1-12

Fig 12A - INCLUSIVE OR-gate circuit

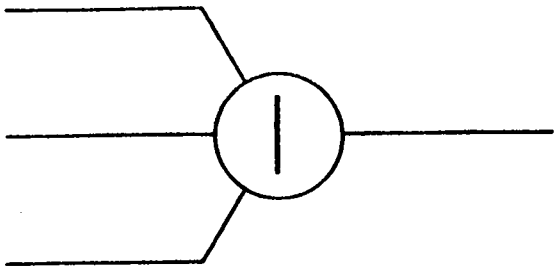


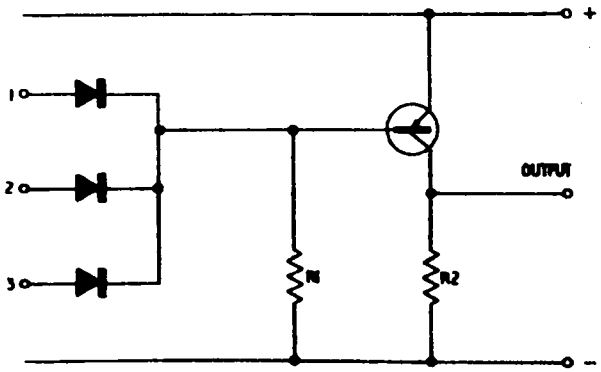
Fig 12B - INCLUSIVE OR-gate logic symbol

NOR-gate

(Fig 13)

28. A NOR-gate will only produce an output when all inputs are absent.

29. In the no signal state, the inputs are negative so that the diodes are not conducting. The transistor is biased on by base current flowing through R1. A positive signal applied to point 1, 2 and 3 will be conducted through one of the diodes, making the transistor base positive. This will reduce the current flowing through the transistor, and hence through R2. Thus if one or more of the inputs are energised, the positive output condition will cease to exist.



T A 339 / 1-13

Fig 13A - NOR-gate circuit

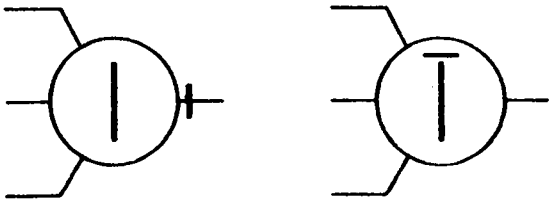


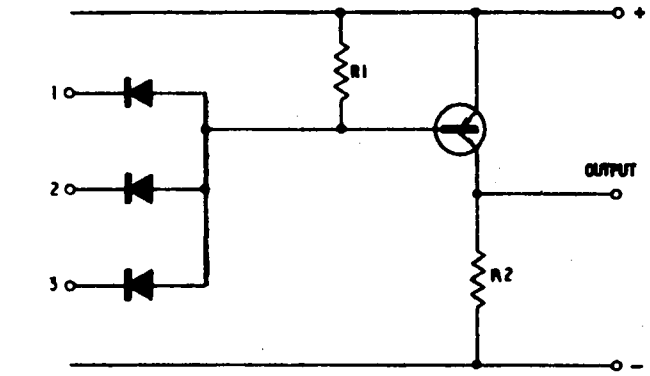
Fig 13B - NOR-gate logic symbols

NOT AND-gate

(Fig 14)

30. A NOT AND-gate (or NAND-gate) will only produce an output when at least one input is absent.

31. In the no signal state, the inputs are negative so that the diodes are conducting, and the transistor is biased on. A positive signal applied to point 1, 2 or 3 will bias the appropriate diode into non-conduction but will make no significant difference to the current flowing through the transistor. If positive signals are applied to points 1, 2 and 3, simultaneously, all the diodes will be reverse biased and the transistor will cease to conduct for the duration of the signals. Thus if all inputs are energised, the positive output condition will cease to exist.



T A 339 1-14

Fig 14A - NOT AND-gate circuit

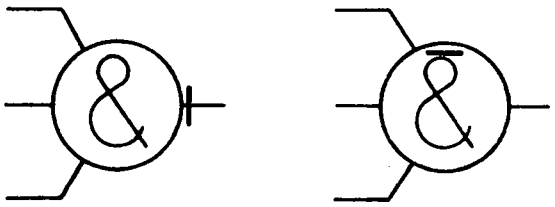


Fig 14B - NOT AND-gate logic symbols

AND-gate using mixed logic

(Fig 15)

32. Sometimes it is necessary to operate a gate with input signals of different polarities. Fig 15 shows a typical circuit and switching waveform for an AND-gate working with one negative and two positive input signals.

33. In the no signal state, inputs 2 and 3 are negative so that R1 is effectively short-circuited and there can be no output from VT1. If a negative signal at input 1 is coincident with positive signals at inputs 2 and 3, then VT1 will be switched on at the same time as the two diodes are reverse biased. An output signal will appear on the base of VT2, switching VT2 off, for a time interval equal to the time of input signal coincidence.

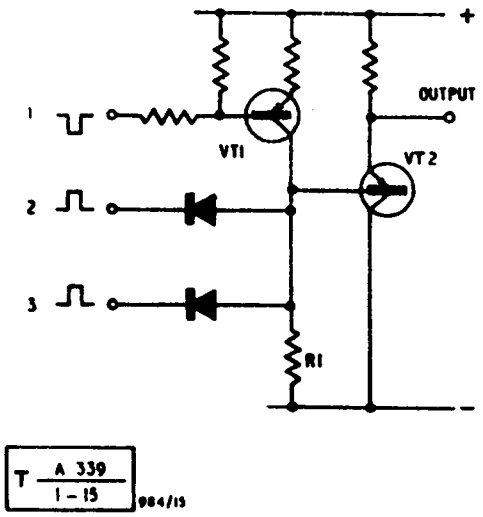


Fig 15A - Circuit of AND-gate using mixed logic

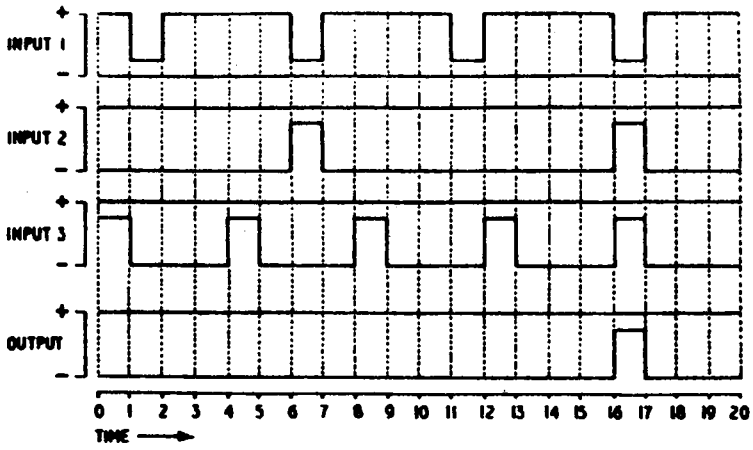


Fig 15B - Waveforms of AND-gate using mixed logic

NOR-gate with active inputs

(Fig 16)

34. For some purposes it is convenient to construct a NOR-gate using one transistor for each input.

35. In the no signal state, the inputs to the transistor bases are negative, so that the transistors are biased on. The output point is thus positive with respect to earth. If one of the inputs is made positive, the appropriate transistor will be biased into non-conduction. The output will however, remain positive because the other transistors are conducting and causing a voltage to appear across R1. If all the inputs are made positive together, the transistors will all become biased off, current will no longer flow through R1, and the positive output condition will cease to exist.

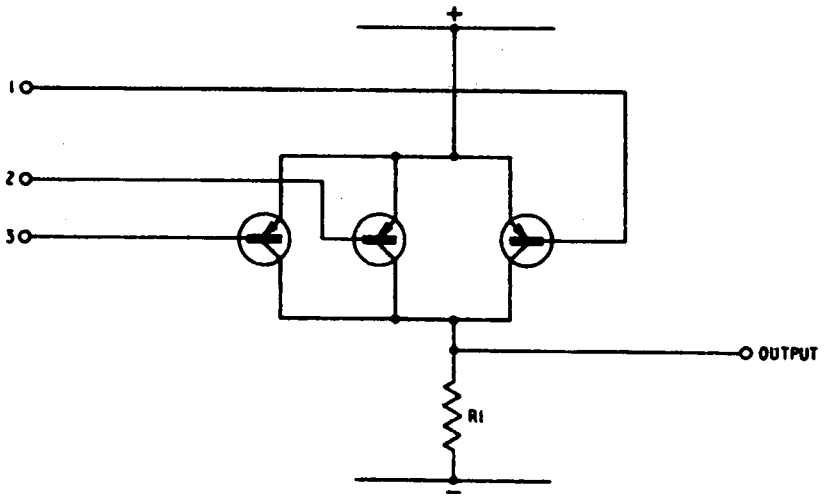


Fig 16 - Circuit of NOR-gate with active inputs

EXCLUSIVE OR gate

(Fig 17)

36. An EXCLUSIVE OR gate (or NON-EQUIVALENCE gate) has two inputs only, and performs the logic function Modulus 2 addition. The output condition occurs when a signal is present at only one input point. The logic symbol is shown in Fig 17B.

37. A typical circuit for carrying out this operation is shown in Fig 17A. When the two inputs are negative both VT1 and VT4 will conduct and current flows through R1, R2, R3 and through R4, R5, R6. This causes VT2 and VT3 emitters to become positive with respect to their bases, so that VT2 and VT3 are biased off, and no output pulse appears across R9. When both inputs are positive VT1 and VT4 are biased off and VT2 and VT3 emitters and bases are at approximately the same potential and again no output pulse appears across R9. When the inputs are dissimilar, ie positive and negative or negative and positive, VT1 (or VT4) will be biased off and VT4 (or VT1) will conduct. The voltage drop across the emitter loads of whichever transistor is conducting will result in either VT2 or VT3 conducting, while the other is biased off. The conducting transistor, VT2 or VT3, will cause an output pulse to appear across R9. Diode MR1 in conjunction with the potential chain R7, R8, maintains a fixed potential at the output for the no signal condition.

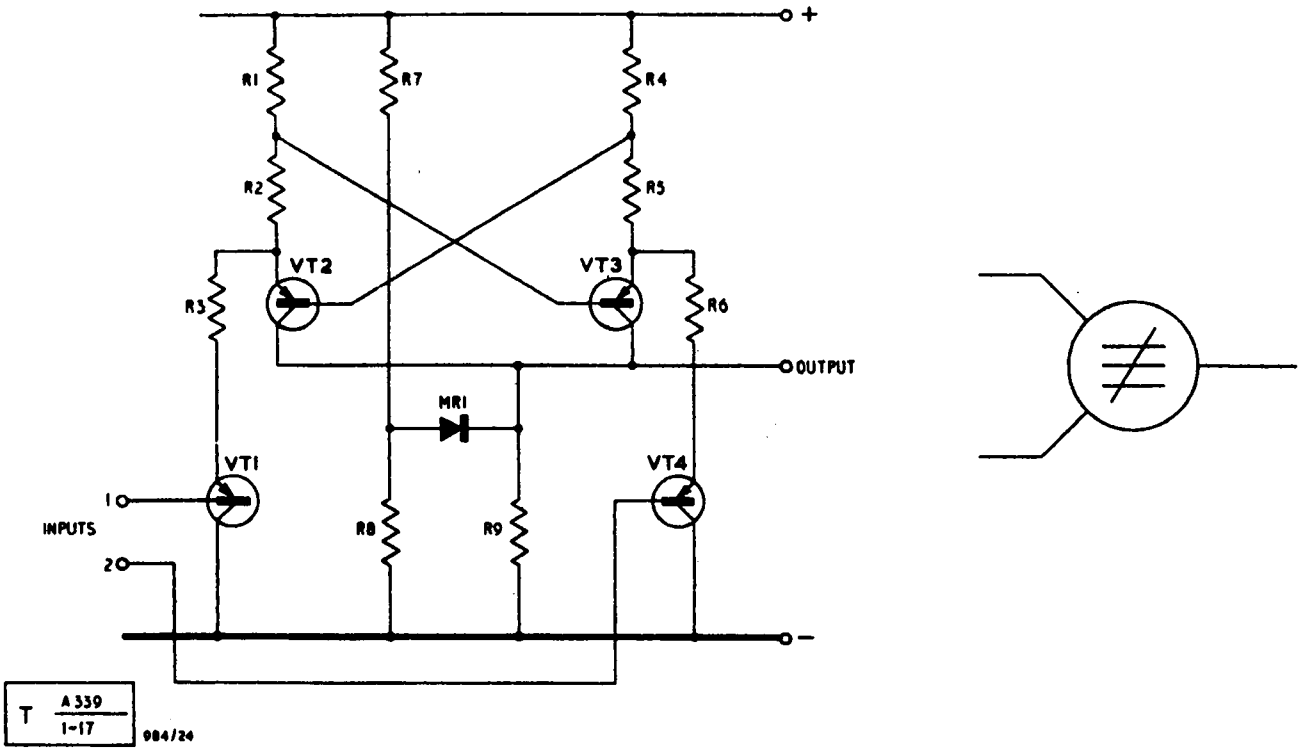


Fig 17A - EXCLUSIVE OR-gate circuit Fig 17B - EXCLUSIVE OR-gate logic symbol

PULSE PLUS BIAS - gate

(Fig 18)

38. A gate circuit may employ PULSE PLUS BIAS operation. This method uses input signals which are individually of insufficient amplitude to operate the gate. If two or more signals coincide however, the resultant amplitude will operate the gate and perform the required logic function. This method is sometimes used when a particular operation has to be performed by a short synchronous (clock) pulse in combination with a bias signal of comparatively long duration. The waveform of such an arrangement is shown in Fig 18.

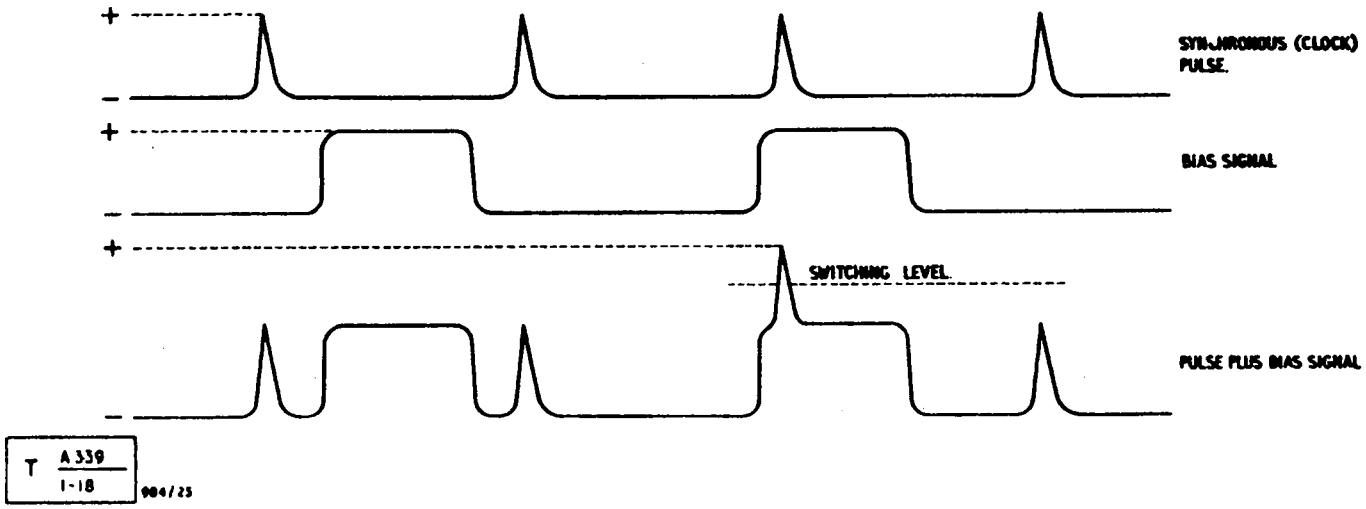


Fig 18 - PULSE PLUS BIAS - gate waveforms

SIGNAL PROCESSING CIRCUITS

BINARY COUNTER

39. A binary counter circuit is a frequency divider in which the input p.r.f. is halved by each successive stage. It is common practice to use a series of bistable stages as shown in Fig 19. The bistable circuit is described in para 10-14.

40. A signal of frequency n c/s applied to the input, causes a signal of n/2 c/s to emerge from the first stage and a signal of n/4 c/s to emerge from the second stage. This process continues progressively through successive stages.

41. In practice, such a circuit could be used to provide synchronous submultiples of time signals which would be applied to the input as a train of rectangular pulses. Alternatively, it could be used to count a series of pulses applied to the input, presenting the total in binary form.

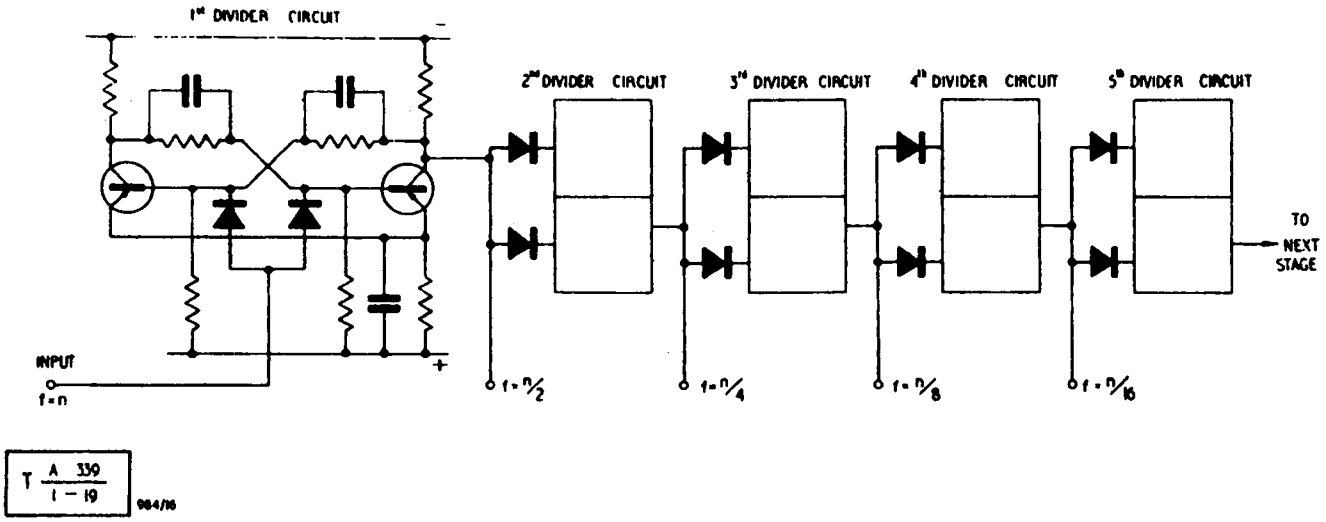


Fig 19 - Binary counter circuit

DECADE COUNTER

General

42. A decade counter gives an output signal at every tenth input signal. The counter shown in Fig 20 employs four bistable stages, with a gating circuit interposed between the first and second stages. Each bistable stage operates as a binary divider circuit.

43. When a signal appears at the counter output, the base of VT2 is made negative and it conducts. Under these conditions, the voltage drop across VT1 and VT2 is very small, and signals applied to the base of VT1 produce no significant output. The first and second divider circuits are thus effectively isolated while the counter gives an output signal.

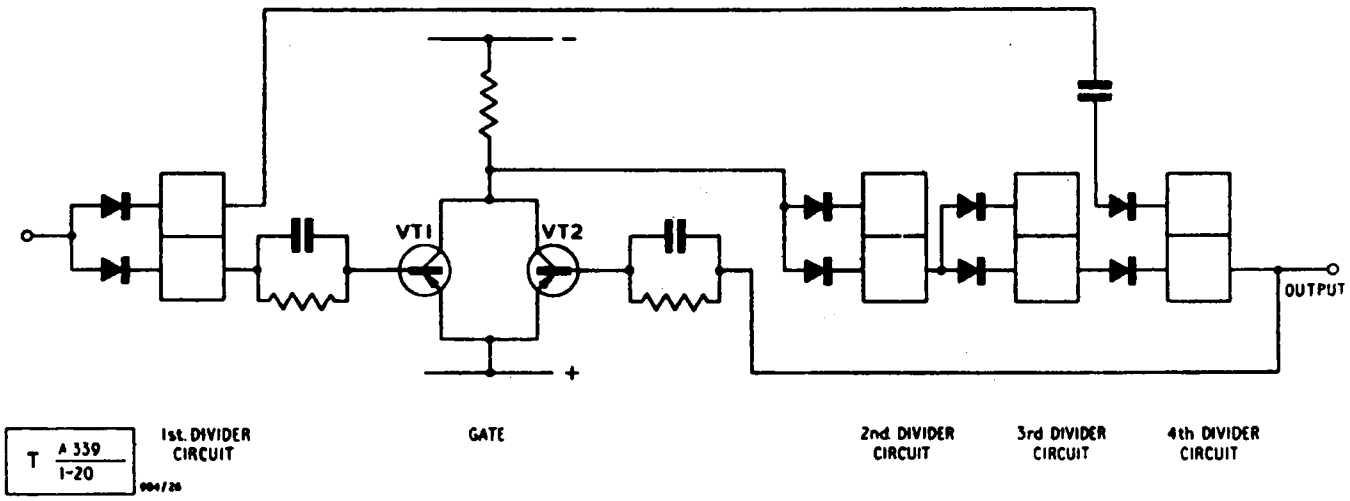


Fig 20 - Decade counter circuit

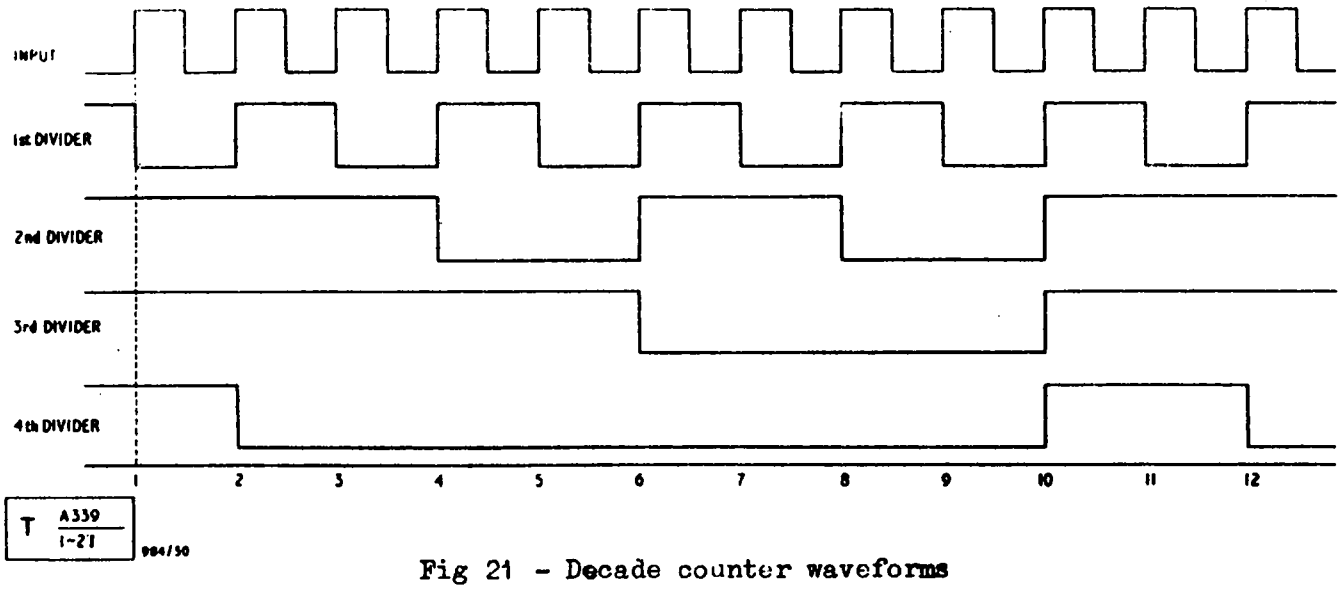


Fig 21 - Decade counter waveforms

Operation

44. The waveforms corresponding to the operating sequence, are shown in Fig 21. In the initial state, an output is present, VT2 is conducting, and the second divider circuit can receive no signals.

1st input - first divider stage changes state
2nd input - first divider stage changes state
fourth divider stage changes state
VT2 biased off, gate 'open'
3rd input - first divider stage changes state
4th input - first divider stage changes state
second divider stage changes state
5th input - first divider stage changes state
6th input - first divider stage changes state
second divider stage changes state
third divider stage changes state
7th input - first divider stage changes state
8th input - first divider stage changes state
second divider stage changes state
9th input - first divider stage changes state
10th input - first divider stage changes state
second divider stage changes state
third divider stage changes state
fourth divider stage changes state
VT2 biased on, gate 'shut'
11th input - first divider stage changes state
12th input - first divider stages changes state
fourth divider stage changes state
VT2 biased off, gate 'open'.

45. From Fig 21 it can be seen that two input signals occur during one output signal. Eight input signals occur between the end of one output signal and the beginning of the next. An input decade is therefore counted between the leading edges (or trailing edges) of consecutive output signals.

GATED DIVIDER

46. A gated divider circuit consists of a sequence of binary counting stages preceded by a gate, such that the dividing operation only takes place when the gate condition is satisfied. Fig 22 shows an AND-gate followed by a 3-stage divider, the object being to provide output signals only if inputs B and C are energised together, and at a particular time. This is achieved by applying to input A, time signals in the form of a train of positive rectangular pulses from a source such as a master clock. If positive pulses appear at inputs B and C at the same time as a pulse appears at input A, a signal will occur at output 1. Because each stage is a binary divider, every second signal at output 1 will appear at output 2, every fourth at output 3 and every eighth at output 4.

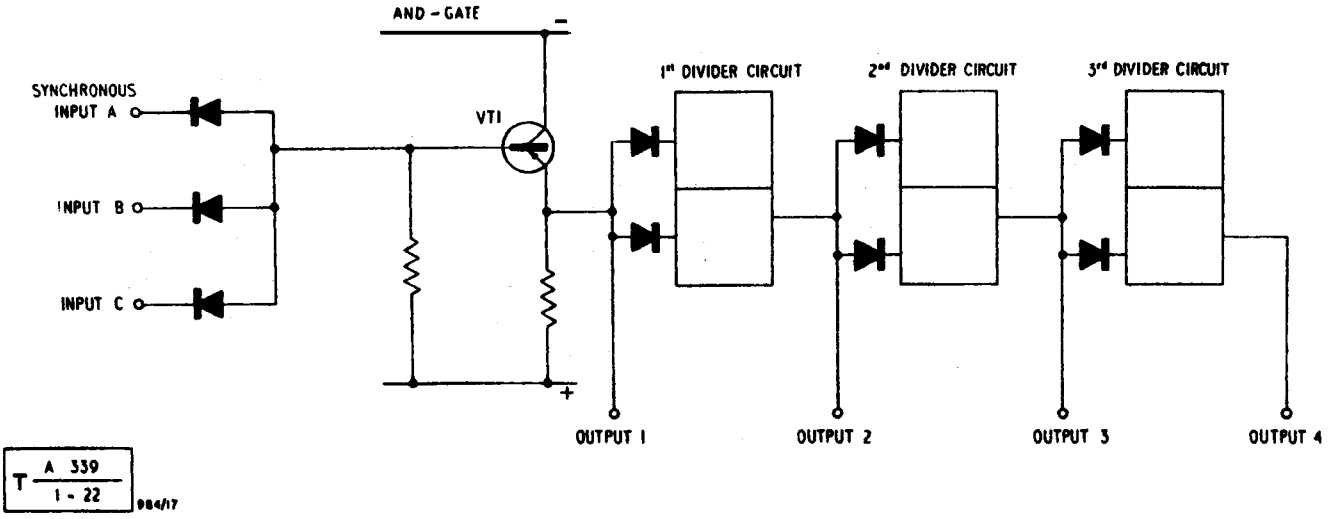


Fig 22 - Gated divider circuit

SHIFT REGISTER

General

47. A shift register consists of a series of bistable elements, connected together by a gating system of diodes. Since a bistable circuit can operate in either of two conducting states, each stage of the register can be made to correspond to either 'MARK' or 'SPACE'. The condition in which any stage is operating may be detected by the voltage level at the collector of either transistor in the bistable circuit.

48. Information in the form of a series of signals is introduced at one end of a shift register and is moved along it, by the application of more information to the input. In practice, the bistable stages and associated gates which make up a shift register, are often operated by a synchronous system such that a 'MARK' or 'SPACE' is applied in conjunction with a time (or clock) pulse. Information therefore advances along the register at a fixed rate.

49. Fig 23 shows representations of a bistable element in 'MARK' and 'SPACE' states, and also a diagrammatic shift register receiving an input of 'MARKS' and 'SPACES' in arbitary sequence. Six consecutive operations are shown, each corresponding to one time pulse. For clarity, gates and interconnections have been omitted.

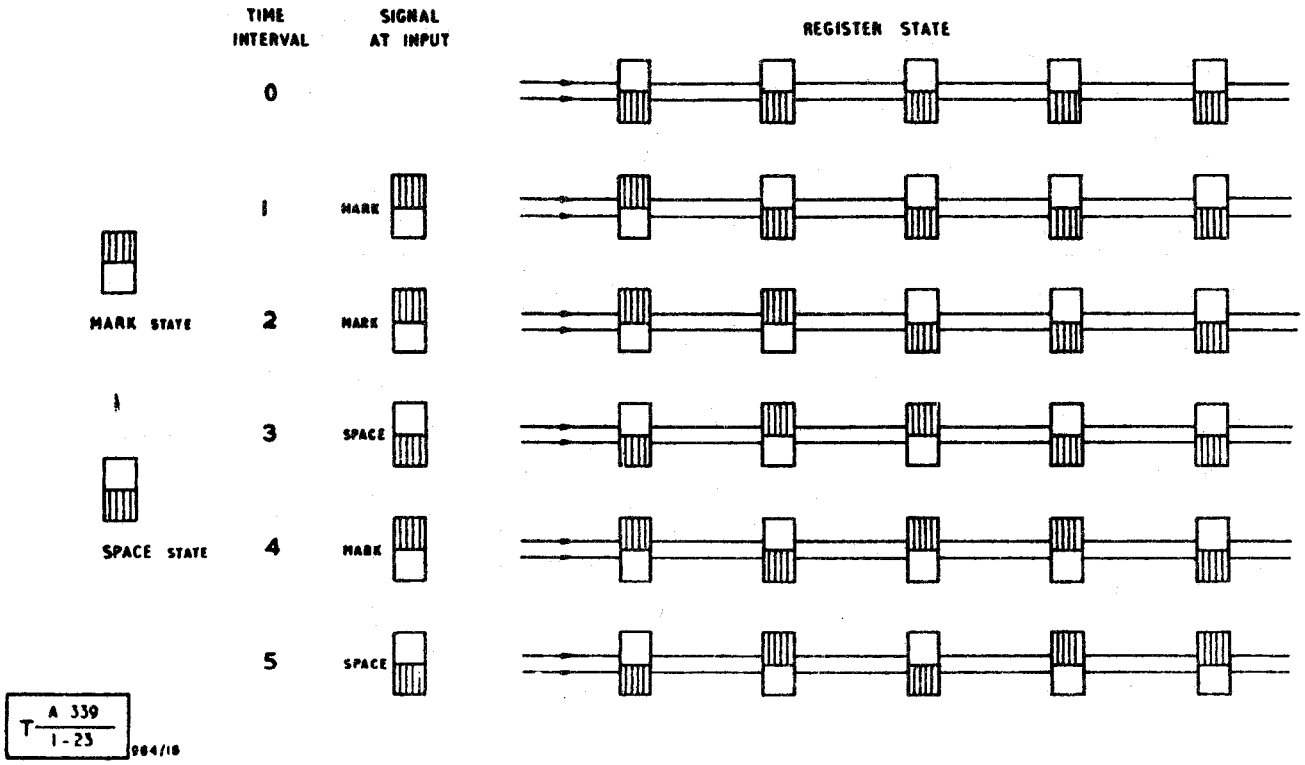


Fig 23 - Diagrammatic shift register

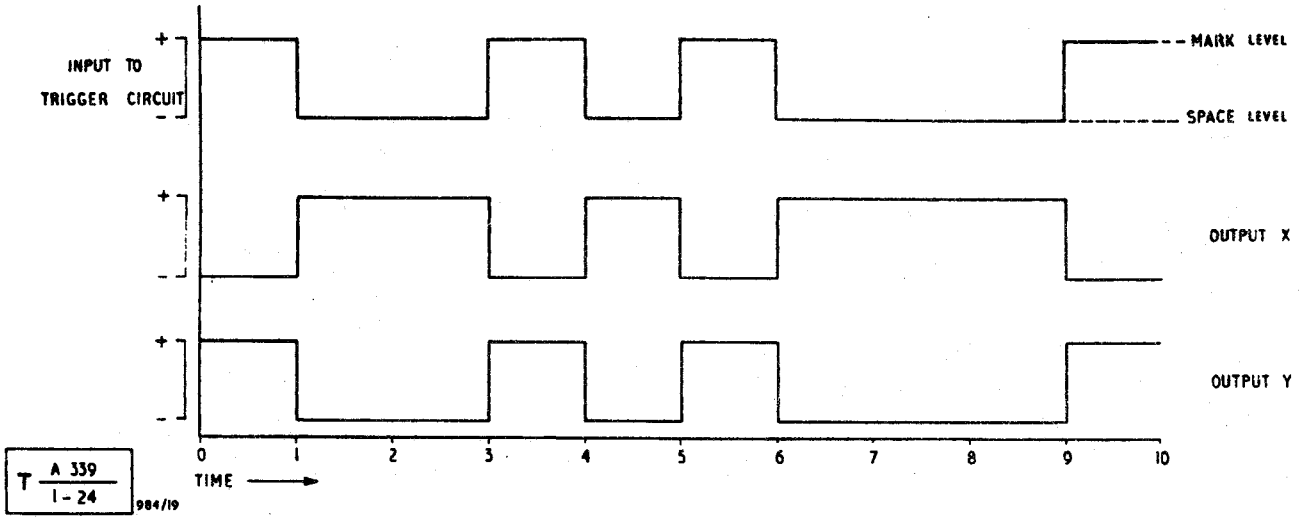


Fig 24 - Shift register drive waveforms

50. Drive for a shift register may be provided by a Schmitt trigger circuit which gives two outputs of equal and opposite polarity. Idealised drive wave forms are shown in Fig 24, the two Schmitt trigger outputs being designated, X and Y. The sequence is arbitrary. The Schmitt trigger circuit is described in para 15-20.

51. Three stages of a shift register are shown in Fig 25, but since all the stages are identical, component values and method of operation are given only for one stage.

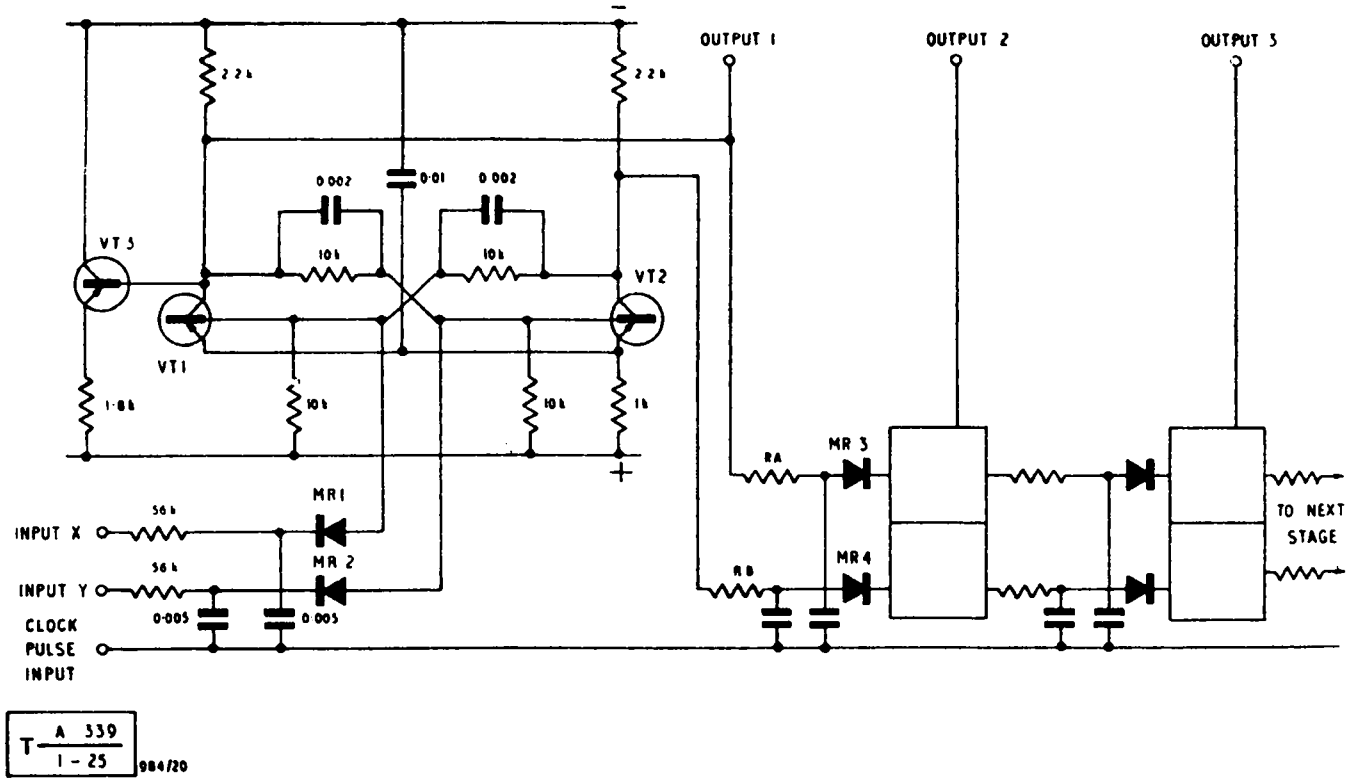


Fig 25 - Three stages of a shift register circuit

Operation

52. Bias levels are chosen such that diodes MR1 and MR2 are back biased by an amount greater than the amplitude of any of the signals which are applied to inputs X and Y. The bistable circuit is thus effectively isolated from input signals. When a positive signal coincides with a clock pulse, the resultant voltage is greater than the diode back bias and the bistable circuit receives a trigger pulse. A 'MARK' is represented as a positive signal at one input, whilst a 'SPACE' is represented as a positive signal at the other input, (see Fig 24) so that the bistable circuit conducts in one state when a 'MARK' signal is received, and in the other state when a 'SPACE' signal is received. When VT1 is conducting, VT1 collector will be more positive than VT2 collector, and when VT2 is conducting, these conditions will be reversed.

53. The voltage levels at the two collectors thus represent either a 'MARK' or a 'SPACE' condition, and are applied to the gate of the subsequent stage through resistors RA and RB. Since diodes MR3 and MR4 are back biased, the following stage does not receive a trigger signal until a clock pulse is received. When a clock pulse is applied to MR3 and MR4, the diode with least back bias, conducts, and triggers the following bistable circuit. The bistable circuit then assumes a conducting state identical to that previously held by the stage in front. The clock pulse appears at each gate simultaneously, so that the stage-to-stage transfer of information along the register, also takes place simultansously. The outputs shown in Fig 25 are points at which the conducting states of the appropriate stages may be detected. VT3 in Fig 25, prevents large random variations in the 'MARK' and 'SPACE' levels at output 1.

DC/DC CONVERTER CIRCUITS

General

54. A dc/dc converter gives a d.c. output at a particular voltage, from a d.c. input at a different voltage. Units providing h.t. supplies (typically 350V) can operate from low voltage primary or secondary cells, and may achieve efficiencies of 80°/o to 90°/o. Most practical circuits employ a push-pull square-wave oscillator which chops the d.c. input. The resultant rectangular waveform is fed to a transformer of the required ratio, after which, it is rectified and smoothed. Fig 26 shows a basic push-pull square-wave oscillator circuit.

Operation of push-pull square-wave oscillator

55. In Fig 26, the transistors are operating virtually as switches, and T is a saturating transformer. When the circuit is switched on, the transistor in the highest gain condition, will conduct.

Assume VT1 conducting
Current through VT1, energises T
T gives forward bias to VT1 base
and reverse bias to VT2 base
VT2 cut off
current increases through VT1
transformer reaches saturation
voltage across VT1 collapses
base drive to VT1 reduced
feedback biases VT1 off
stored energy in T drives VT2 on
VT2 conducts.

56. This cycle is then repeated in the reverse direction. An alternating flux is thus set up in the transformer, causing an alternating voltage to appear across the output winding.

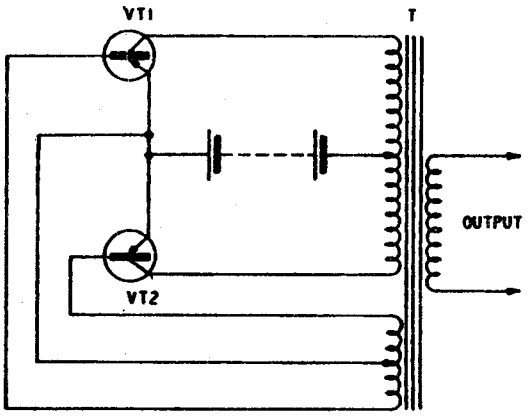


Fig 26 - Push-pull square-wave oscillator circuit

Practical dc/dc converter circuit

57. In practice, a circuit such as the one shown in Fig 26 would have unreliable starting characteristics, since the transistors are biased close to cut-off. This difficulty is often overcome, by placing sufficient resistance in the base circuit, to provide starting bias. In order to avoid excessive reduction of converter efficiency, resulting from power dissipated in the base circuit resistance, a diode may also be provided in the base circuit. The diode provides a low resistance conduction path for the much larger base current which flows when the system is oscillating. Fig 27 shows the circuit of a practical dc/dc converter, capable of providing H.T. and L.T. supplies for telecommunications equipment.

58. From the basic circuit in Fig 26, it can be seen that the transistor which is cut-off, is subjected to twice the supply voltage. For this reason, the unit shown in Fig 27, employs two transistors in series, in each side of the oscillator; thus ensuring that the voltage across a transistor which is cut-off, never exceeds the supply voltage.

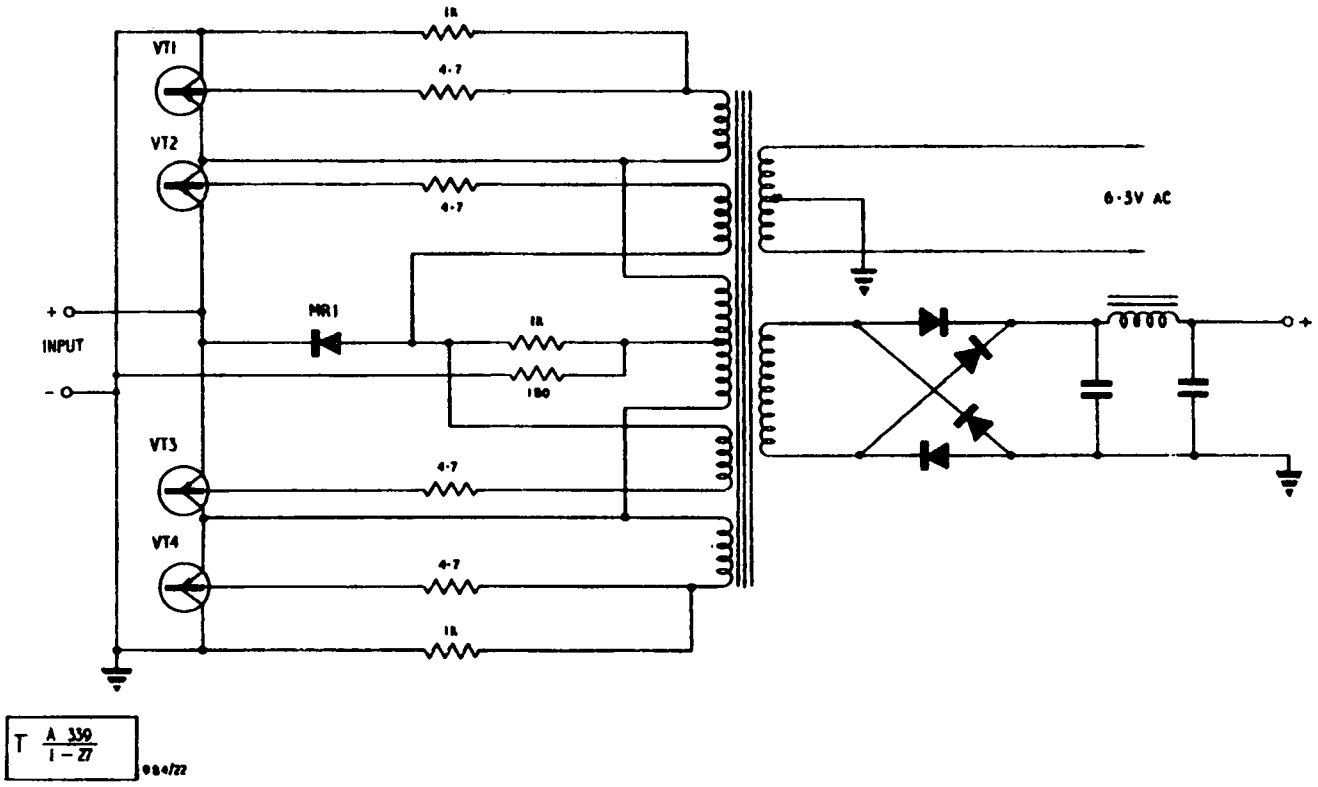


Fig 27 - Practical dc/dc converter circuit

EME8/8a/984

END